

REMARKS

Claims 1-7 and 9 have been rejected under 35 USC 103(a) as unpatentable over Akatsu in view of Chudzik. The rejection is respectfully traversed.

The present invention discloses a method of producing a deep trench capacitor in a semiconductor substrate with an improved aspect ratio and improved capacitance. In this regard, the claimed invention (as amended) requires depositing a very thin conformal aluminium-oxide layer in the first trench for shielding the side walls of the first trench, wherein the very thin conformal aluminum-oxide layer provides a process window which is as wide as possible for processing a second trench underneath the first trench. This added feature is disclosed, for example, in the original specification on page 4, lines 16-23 and page 8, lines 8 and 9. Akatsu, on the other hand, discloses use of a nitride layer as a shield for the side walls of the trench (col. 8, lns. 25 ff.).¹

Additionally, the Examiner states that “Akatsu further discloses that the layer 660 is made of a dielectric material such nitride later. However, aluminum oxide may be used to replace the nitride layer since aluminum had higher dielectric constant which is a factor that provides higher capacitance[.]” but that “it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use a well known high-k dielectric material as taught by Chudzik in order to take the advantages as mentioned above.” Applicant’s respectfully disagree. Specifically, the dielectric layer 400 disclosed in Chudzik, at paragraph [0010], does not show a shielding function. The dielectric layer 400, e.g. Al_2O_3 functions as a dielectric for the capacitor. Hence, Chudzik does not disclose or suggest using Al_2O_3 for shielding the side walls of a trench. Moreover, Chudzik discloses a thick dielectric formed in a trench along side wall 210 (paragraph [0009]).

The present invention advantageously discloses conformal aluminium-oxide layer providing a process window which is as wide as possible for processing the second trench underneath the first trench. Thus, the volume of the capacitor built in the deep second trench is increased which follows a higher capacitance of the capacitor. The increase in the capacitance of

¹ It appears the Examiner mistakenly cites Chudzik, as opposed to Akatsu, when commenting on the rejection in paragraph 2 of the Office Action. Applicant’s proceed accordingly.

the trench does not enlarge the surface occupied by the memory cell. Therefore, at a predetermined integration degree, the capacitance of the capacitor can be increased or at a predetermined capacitance the integration degree of the memory cell can be increased.

Since the recited method is not disclosed by the applied prior art (either alone or in combination), claim 1 is patentable. Claims 2-7 and 9, depending from claim 1, are similarly patentable.

Claim 8 has been rejected under 35 USC 103(a) as unpatentable over Akatsu and Chudzik as applied to claims 1-7 and 9. The rejection is respectfully traversed for the same reasons presented in the arguments above.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 543822005300.

Dated: April 6, 2006

Respectfully submitted,

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